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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,462	10/20/2003	Wen-Ting Chu	N1085-00156	4151

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EXAMINER	
ECKERT II, GEORGE C	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 06/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/689,462	CHU ET AL.
	Examiner	Art Unit
	George C. Eckert II	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) *14-33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/20/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 14-22 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on March 30, 2005.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they **do not include** the following reference sign mentioned in the specification: STI structures 403.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they **include** the following reference characters not mentioned in the description: none of the numerals used in figure 3 are described in the specification (e.g. 300, 310, 320, 330 and 340).

4. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

5. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-3 and 5-13 are rejected under 35 U.S.C. 102(e) as being anticipated by 6,800,525 to Ryu et al. Ryu et al. teach, with reference to figures 2e-2o, a method of making a split gate field effect transistor comprising:

providing a substrate 200 having a pair of floating gates 211, a first conductive material layer 209 between the floating gates, and a first dielectric layer 217 above the first conductive material layer;

forming a control gate 219 having a second dielectric layer 217 above the control gate, wherein the control gate is self-aligned to the floating gates by using the first and second dielectric layers as an etching hard mask (figs 2k-m and col. 5, lines 38-44); and

forming a pair of source/drain regions 224 (fig. 2o) into the substrate and beside the pair of floating and control gates.

Regarding claims 2, 3 and 5, Ryu et al. teach that the first and second dielectric layers 217 are formed by thermal oxidation (col. 5, lines 27-30, and line 2 teaching the oxidation process may be a thermal oxide) and are thicker in the middle than on an edge (fig. 2k).

Regarding claim 6, Ryu et al. teach the method further comprising:

forming a second conductive material layer 214 above the substrate;

forming a hard mask layer 215 above the second conductive material layer;

removing portions of the hard layer and the second conductive layer (figs. 2h and 2i);

forming the second dielectric layer 217 above the second conductive layer (fig. 2k); and

removing a remaining portion of the hard mask layer 215 and an additional portion of the second conductive material layer 214 by using the first and second dielectric layer as an etching hard mask (col. 5, lines 38-44).

Regarding claim 7, Ryu et al. teach that the second dielectric layer 217 is formed using the hard mask layer 215 as an oxidation resistant layer (col. 5, lines 26-30). Regarding claim 8, Ryu et al. teach that the hard mask layer is silicon nitride (col. 4 line 67).

Regarding claim 9, Ryu et al. teach that the step of removing the hard mask and second conductive material comprises:

forming a sacrificial layer 216 above the hard mask (fig. 2g);

removing portions the sacrificial layer 216, the hard mask 215 and the second conductive layer 214 (fig. 2h);

removing a remaining portion of the sacrificial layer (fig. 2k).

Regarding claim 10, Ryu et al. teach that the sacrificial layer 216 is used to planarize a surface of the substrate (fig. 2i). Regarding claims 11-13, Ryu et al. teach that the sacrificial layer may be an HDP-CVD film (organic), which may function as a photoresist, or a USG (spin on glass) layer (col. 5, lines 9-12).

7. Claims 1-8 are rejected under 35 U.S.C. 102(e) as being anticipated by 6,706,592 to Chern et al. Chern et al. teach, with reference to figures 3k-3q, a method of making a split gate field effect transistor comprising:

providing a substrate 10 having a pair of floating gates 14, a first conductive material layer 58 between the floating gates, and a first dielectric layer 60 above the first conductive material layer;

forming a control gate 70 having a second dielectric layer 68 above the control gate, wherein the control gate is self-aligned to the floating gates by using the first and second dielectric layers as an etching hard mask (col. 6, lines 40-42); and

forming a pair of source/drain regions 76 into the substrate and beside the pair of floating and control gates.

Regarding claims 2-5, Chern et al. teach that the first 60 (col. 6, line 9) and second 68 (col. 6, line 37) dielectric layers are silicon oxide, that the second layer 68 is formed by thermal oxidation (col. 6, line 39) which inherently has a thicker middle portion (e.g. birds beak when formed using a surrounding nitride mask as here) and that the silicon oxide has a thickness of 8 to 80 nm (80 to 800 Å).

Regarding claim 6, Chern et al. teach the method further comprising:

forming a second conductive material layer 62 above the substrate;

forming a hard mask layer 64 above the second conductive material layer;

removing portions of the hard mask layer and the second conductive layer (fig. 3n);

forming the second dielectric layer 68 above the second conductive material layer (fig. 3p); and

removing a remaining portion of the hard mask layer 64 and an additional portion of the second conductive material layer 62 by using the first and second dielectric layer as an etching hard mask (col. 6, lines 39-47).

Regarding claim 7, Chern et al. teach that the second dielectric layer 68 is formed using the hard mask layer 64 as an oxidation resistant layer (col. 6, lines 37-39). Regarding claim 8, Chern et al. teach that the hard mask layer 64 is silicon nitride (col. 6 line 15).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The additional cited art teaches methods of making EPROM devices using an oxide layer as a mask over an aligned control gate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George C. Eckert II whose telephone number is (571) 272-1728.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax number is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GEORGE ECKERT
PRIMARY EXAMINER